Graphenea

Measurement Protocols and Handling Instructions

Graphene Field-Effect Transistor Chip:
GFET-S20, S21, S22, S20P, S21P & S22P

Typical Measurement Configurations

The following explains different electrical measurements that can be performed in GFET-S20 chips.

These devices allow field-effect measurements by simultaneously applying two voltages:

- Source-drain voltage (V_{SD}): applied between the two probes (source and drain), while one of them is grounded (see Figure 1a). V_{SD} enables the transport of charge carriers through the graphene channel, with an associated source-drain current (I_{SD}). V_{SD} can be varied in order to get the desired I_{SD} outcome (see Figure 1b).

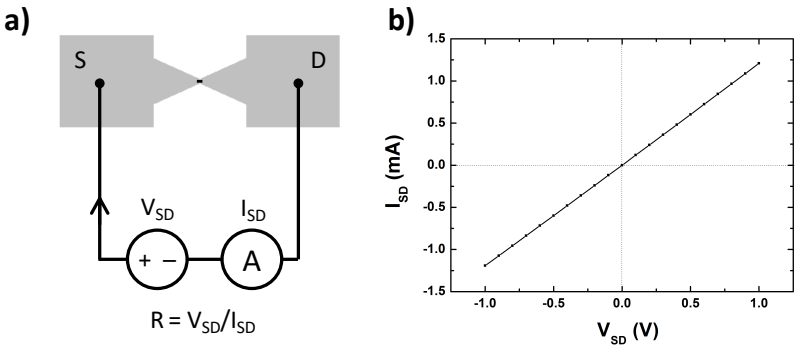

Figure 1. a) Scheme of the 2-probe device, with the corresponding electrical measurement configuration. b) Typical output curve measured at room temperature and vacuum conditions.

- Gate voltage: this voltage can be applied to the silicon (Si) on the substrate (back gating), or to an ionic liquid placed on top of the chip (liquid gating), which will be explained below.

Back gating

Silicon can be contacted from the top surface by scratching the 90 nm-thick SiO_2 with a diamond pen in one of the chip corners; or alternatively from the underside of the chip, for instance using a probe station chuck. Figure 2 shows a typical transfer curve when a gate voltage V_G is applied on the Si.

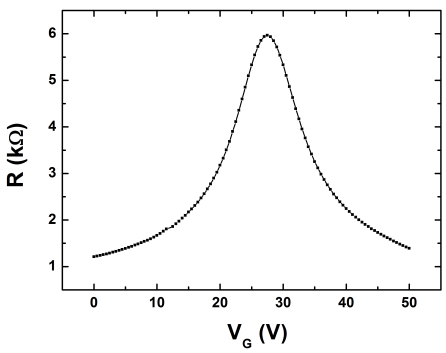

Figure 2. Typical transfer curve of a graphene device, where the device R is measured as a function of the back gate voltage V_G.

From the data in Figure 2, several parameters associated to the graphene can be calculated.

The resistivity of graphene is usually expressed per thickness unit, i.e. the so-called sheet resistance:

$$R_S = R\frac{W}{L},$$

being W and L the width and length of the graphene channel, respectively. The field-effect mobility (μ_{FE}) can be calculated by using the following equation:

$$\mu_{FE} = g \cdot \frac{1}{C_{sio2}},$$

where:

- $g = d\sigma/dV_G$ is the transconductance, being $\sigma=1/R_S$,
- C_{SiO2} is the capacitance per unit area of the 90 nm-thick SiO_2 dielectric.

μ_{FE} is usually calculated using the maximum transconductance. Note that this calculation includes the voltage drop at the graphene/metal interface, therefore μ_{FE} is a lower bond of the intrinsic mobility of the graphene channel.

Liquid gating

Alternatively, the charge carrier density of the graphene can be modified by applying a voltage to an ionic liquid in contact with the device channel. This voltage can applied in two ways:

- By an external electrode immersed in the liquid. Ag/AgCl electrodes are widely used for this purpose.
- By the non-encapsulated electrode located at the central area of the chip (see TDS file).

Figure 3(a) and (b) show typical transfer curves obtained for liquid gating using a Ag/AgCl electrode or the on-chip electrode, respectively. In this case, the Dirac point is observable for much lower liquid gate voltage (V_L) values compared to back gating.

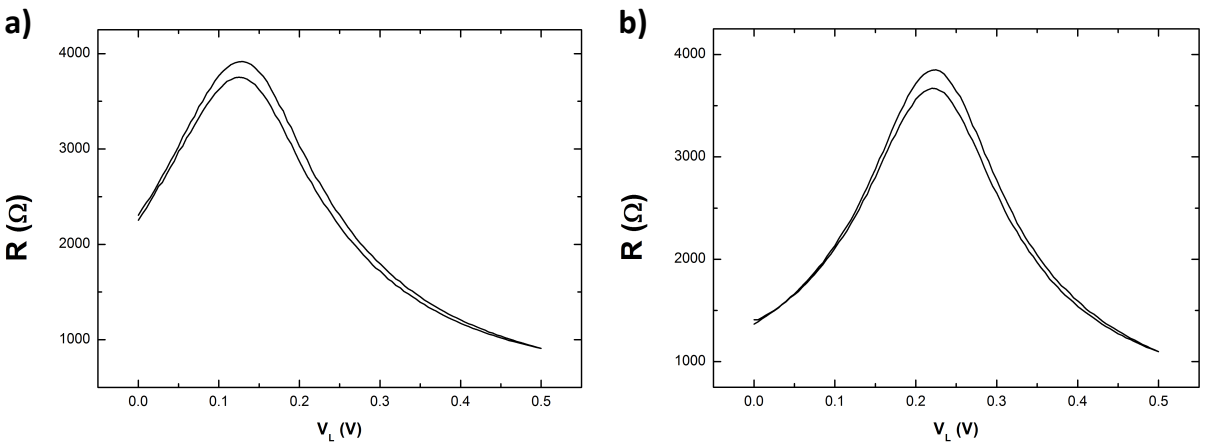

Figure 3. a) Gating through Phosphate Buffered Saline (PBS, pH=7.3), using an external Ag/AgCl electrode. b) Gating through PBS, using the on-chip AuPd electrode.

Doping-reduction treatment

Graphene on SiO_2 is often p-doped after exposure to air due to the adsorption of water molecules and other adsorbates with the effect that the Dirac point is shifted to positive gate voltages and can cause the Dirac voltage to be located out of the recommended gate voltage range, specially during back gate measurements.

Immersing the GFET chip in acetone for at least 12h reduces doping. After that, the chip should be rinsed with IPA, and properly dried with an Ar or N_2 gun. In order to preserve the effectivity of this treatment, electrical characterization should be carried out in inert atmosphere or vacuum. This treatment is specially recommended for measurements in dry conditions, and is not necessary for liquid gating experiments, because the V_L values needed to observe the Dirac point are acceptable even without the treatment.

In addition, storage of the chips in a low humidity environment (N_2 cabinet, desiccator, or vacuum) is highly recommended.

Basic handling instructions

The graphene used in our GFETs is high-quality monolayer CVD graphene and highly prone to damage by external factors. To maintain the quality of your devices, we recommend taking the following precautions:

- Be careful when handling the GFET chip that tweezers do not make contact with the device area. Metallic tweezers should be avoided, as they can damage/scratch the chip edges/surface
- Treat the devices as sensitive electronic devices and take precautions against electrostatic discharge
- Ideally store in inert atmosphere or under vacuum in order to minimize adsorption of unknown species from the ambient air
- Do not ultrasonicate the GFET dies
- Do not apply any plasma treatment to the GFET dies
- Do not subject the GFET dies to strongly oxidizing reagents

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